Design of Improved Ancient Vedic Multiplier Using Verilog

S Praveen Kumar Department of Electronics and Communication Engineering, Saveetha Engineering College,Chennai.

T Aravind Department of Electronics and Communication Engineering, Saveetha Engineering College,Chennai.

Gina S Department of VLSI, Saveetha engineering college, Chennai. gina.s.pandian@gmail.com

Abstract— Currently, the all-processor core will be consolidated into a singular unit owing to the rising requirement for high performance in intricate algorithms and multifunctionality. Nevertheless, the CPU demand is substantial. We should provide copper roses for supportive operations conducted by the primary processor to mitigate it; they will engage with copper roses. Numerical operations, encompassing joint calculations, multiplications, and digital signal processing applications, among others. The velocity of coprocessors dictates the processor's performance. Vedic arithmetic is an ancient kind of calculation characterised by a distinctive methodology of 16 sutras designed to swiftly derive solutions to various practical problems. Vedic sutras, including Urdva Tirkabhyam, and 64-bit aluminium architecture are considerations when contemplating. Vedic formulae pertain to multiplication operations. Vedic formulas significantly assist the enforced arithmetic modules, particularly in instances of delay. Utilising these mathematical principles, we constructed an aluminium model using Verilog HDL and synthesised it in Xilinx ISE; we have determined that it exhibits superior performance.

"Keywords: Vedic math, Cross Multiplication, 64x64 Vedic multiplier, Urdhva-Tiryagbhyam sutra"

I. INTRODUCTION

A fundamental skill for arithmetic operations is multiplication. Currently, intensive arithmetic function calculations (CIAF) involve numerous digital signal processing (DSP) programs, including confusion, fixed Fourier transform (FFT), filtering, and various marginal operations. These tasks are frequently executed on microprocessor units, encompassing multiplication and related operations. Mathematics is essential for serious endeavours, including counting and multiplication, as well as intricate scientific and commercial calculations derived from fundamental daily duties.

Therefore, computers must have a brief and green arithmetic unit. Comparatively to the partial product parallel computing approach, array multiplication requires much less time. The created delay is the time needed for the alerts to flow via the multiplication array gates. massive booth arrays are utilized in booth multiplier designs for exponents computations with high velocity that finally requires partial upload and partial carry registers. wherein ok is the quantity of sales space recorder adder ranges, Utilising an N-bit opening multiplication necessitates a Radix-4 multiplier to attain a portion of the end product in around N-Bits/(2K) clock cycles.

The digital multiplier for the Array multiplier can be constructed via the Urdva Tiryakabhyam Sutra-based "Vertical Crosswiz algorithm." Recall that the minor components of size (n/2 = n) are stated to allow the ancient formula to allocate space for calculating the product of n, with n bits per multiplier. These portions will sustain damage when subjected to a low quantity (N/2 each), typically resulting in 2x2 dimensions. It facilitates jogging in the therapy.

VEDIC MATHEMATICS

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These sources, with their significant meanings, are enumerated alphabetically here.

1) (Anurupye) Shunyamanyat - If one is present, the other is absent.

2) Chalana-Kalanabyham - Distinctions and resemblances.
3) Ekadhikina Purvena - Exceeding the previous amount.
4) Ekanyunena Purvena - Inferior to the preceding one.
5) Gunakasamuchyah - The elements of yoga resemble the yoga of elements.
6) Gunitasamuchyah - The product of yoga is equivalent to the yoga of the product.
7) Nikhilam Navatashcaramam Dashatah - All events commence at 9 and conclude at 10.
8) Paraavartya Yojayet - Convey and modify.
9) Puranapuranabyham - Confirmation of accomplishment or lack thereof.
10) Sankalana-vyavakalanabhyam – Additionally, through subtraction.
11) Shesanyankena Charamena - Remaining Final Digit.
12) Shunyam Saamyasamuccaye - When yoga equates to zero, it is identical to yoga.
13) Sopaantyadvayamantyam - The greatest and twice repeated.
14) Urdhva-tiryagbhyam - Vertical and Crosswiz.
15) Vyashtisamanstih - Part and Whole.
16) Yaavadunam - The extent of its deficiency

4 By Vizadam books, including Vedic mathematics. The event occurs in an elevated (complementary) stopya-bya as described in the Atharva Vedas concerning civil engineering and architecture. It elucidates several mathematical concepts like arithmetic, geometry (aircraft, coordination), trigonometry, quadratic equations, factors, and even stones. In the course of amalgamating these endeavours, his holiness Jagadguru Shankaracharya Bharati Krishna Terathji Maharaja (1884–1960) contested the application and provided a mathematical rationale for it. Following extensive study of the Atharva Veda, the Swamiji formulated 16 sutras and 16 upa-sutras. The present text of the Atharva Veda no longer contains these sutras, as Swamiji has evolved them himself. Vedic mathematics is both logical and a mathematical marvel. that is the purpose it has such a diploma of grandeur; it cannot be disapproved.

II. LITERATURE SURVEY

For most of the modern processors, one of the most sought-after parts is multiplier. the speed of the CPU is about by multiplier pace. thus, a massive speed multiplier is actually essential. This paintings presents a new Multiplication approach based totally on hybrid adder layout, Wallace tree structure, and modified sales space approach. Comparative redesigned booths for distinct multiplier design, minimise the multiplier The quantity of partial products is minimally delayed. The velocity of the Wallace tree signifies more than merely simultaneous incomplete products. In addition to partial products, ADER is essential. The standard velocity of the multiplier configuration will augment if the pace of supplementary operations is accelerated relative to the overall speed. Therefore, the principal objective of this image is to enhance the additive. Maintain the separation of graphic and text files, provided that the text is appropriately written and styled. Employ solely a hard return at the conclusion of a paragraph; refrain from utilising a hard tab. Upload any type of side documentation at any location inside the work. Text head templates will be created for you; now, there is a lack of variation.

The multiplier design makes gain of a new hybrid adder layout, which reduces vicinity occupied and put off. Stated are the area, put off, and electricity complexity of the counseled Multiplier design. reduced region overhead and important course delay are blessings of The proposed improved multiplier configuration, which demonstrates superior performance compared to the contemporary technique, utilises forward assistance. Utilise Xilinx ISE 10.1 design tools to synthesise the proposed multiplier design using Model Glue 15.7g. Verilog HDL is the utilised programming language.

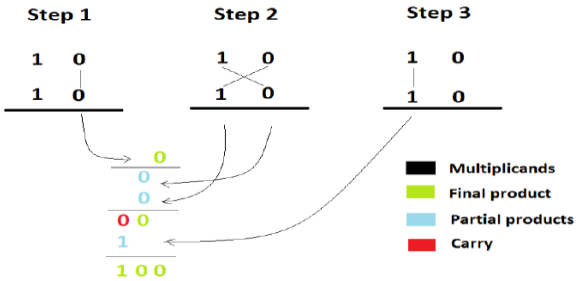
Vedic mathematics is a discourse attributed to ancient Indian systems of arithmetic, originating in the early twentieth century from the ancient Indian scriptures known as the Vedas. It on the whole addresses Vedic mathematical formsulae and their software to other fields of arithmetic. Vedic Sutras help one to simplify or even maximise the algorithms grounded on traditional mathematics.

Trigonometry, simple and spherical geometry, conifers, stones (including both distinctions and significance), and various branches of mathematics can all be directly handled utilising these methodologies and concepts. Based on traditional Indian Vedic Mathematics, novel multiples and class structures are proposed for this endeavour aimed at low energy and rapid applications. It is devoted to all partial products and their monetary creation. The design performance of the Altera Cyclone-II FPGA indicates that the suggested Vedic multiplier and rectangular array multiplier outperform the standard multiplier in speed.

Vedic mathematics refers to the ancient Indian system of arithmetic established in the early 1900s. Vedic mathematics primarily relies on 16 concepts known as sutras. We manage the prospective application of virtual

character treatment for digital assets concerning virtual signage treatment for wood multiplication algorithm software. A fundamental digital multiplier, known as the Vedic Multiplier, is predicated on the Urdhwa Tirikabhama (vertical and crosswise) design. In ancient India, this formula was commonly employed to rapidly multiply two decimal integers. This task shows the formula clearly, after which it is applied to binary quantity systems to enhance its utility in virtual hardware. The hardware design of the Vedic multiplier has been completed and is recognised as the most prevalent array multiplier. If meticulously identified, the Vedas can yield several technical applications from their reservoir of knowledge.

The traditional Indian gadget of arithmetic unearthed in early 20th century is known as Vedic mathematics. 16 principles, sometimes known as word-formulae, are the foundation of Vedic mathematics. We consider a likely utilization of Vedic arithmetic for digital Implementation of the Vedic multiplication method for digital multipliers. Urdva is a principal virtual multiplier, articulated through the Tiriyakhambha (Vertical and Movement Smart) formula, recognised as a Vedic multiplier. Initially, two decimal values were employed for multiplication, a method utilised in ancient India. This artwork gently provides the formula, after which the binary quantity discloses its application within the system's virtual hardware. The hardware configuration of the Vedic multiplier is presented and demonstrated to be the most often utilised array multiplier. If accurately identified, it is highly probable that several analogous technological packages originate from the repository associated with the Vedas.



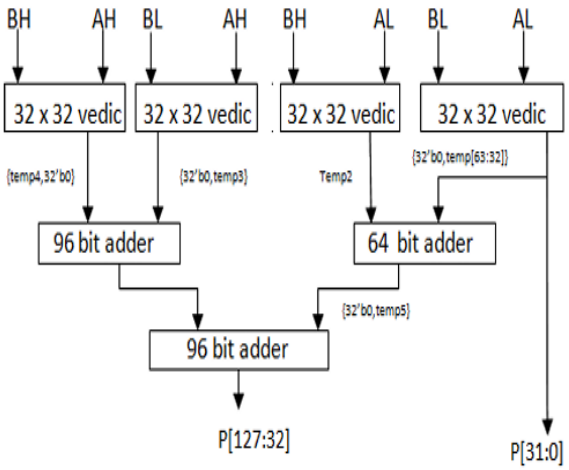
"Fig 1: Cross Multiplication"

The historical subject of mathematics known as Vedic arithmetic uses a unique method of computation grounded on sixteen Sutras. Using these approaches in the coprocessor's computation methods will help to decrease place, electricity, complexity, execution time, etc. Although several sutras are used to address various numerical units, investigating every one yields fresh findings. Our research has demonstrated the efficacy of the Vedic multiplication technique, indicating that the approach employed influences the outcome of multiplication. It employs the Karatsuba algorithm for compatibility across diverse data, which is optimised to minimise multiplication stages by zero and at elevated bit levels, hence facilitating the parallel generation of intermediate products. An energy-efficient multiplier operating at high speed in Coopose should be derived using this formula.

III. PROPOSED DESIGN

Like the 32x32 multiplier, the design of a 64x64 multiplier uses a hierarchical and modular method; but, scaled to fit 64-bit inputs. It makes advantage of the simplicity and natural parallelism of the Urdhva Tiryakbhyam Sutra derived from Vedic mathematics. For high-speed multiplication this technique ensures scalability, efficiency, and great use of assets.

Each enter pair is handled by a separate 32x32 Vedic multiplier built in a fashion akin to lesser multipliers. Calculating the partial products in parallel the use of the Urdhva Tiryakbhyam sutra produces 16 partial product rows usual. to reveal the vertical and pass-product phrases inherent in the Vedic multiplication method, the resultant partial products are oriented vertically and crosswise. Powerful sum of the partial products is carried out with a 64-bit Adder. huge bit-width operations with low put off allow the adder to be selected for managing, consequently optimising the addition process. These partial products taken together offer the multiplier's ultimate 64-bit output.



"Fig 2. Proposed 64-bit Vedic multiplier"

Arranging 32x32 blocks in an green manner basically builds the 64x64 multiplier. Originally created

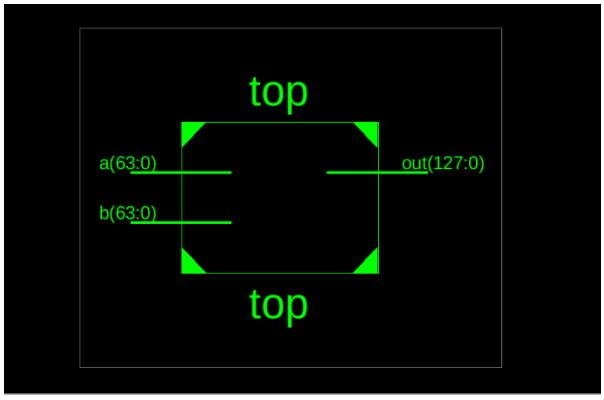
from 8x8 blocks and smaller gadgets, those blocks are themselves built using 16x16 multipliers. Smaller pieces are mechanically reused, as a result this hierarchical method ensures scalability and streamlines the design process.

KEY FEATURES OF THE DESIGN

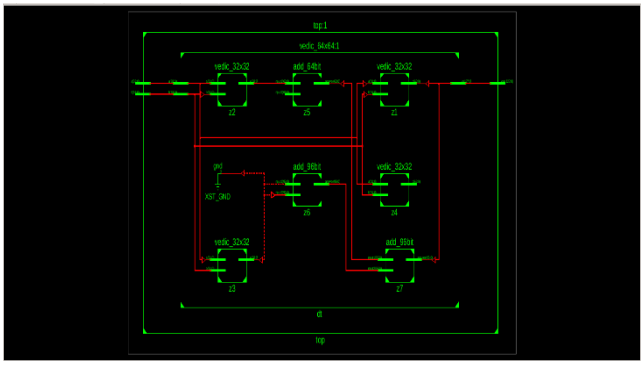
- Dividing the 64-bit inputs into smaller blocks allows partial products to be done in parallel, hence greatly lowering computing time.
- The modular design lets the multiplier be stretched for even more bit-widths without major redesigning work.
- Redundant calculations are avoided and effective logic is used to decrease power usage.
- Parallel computing and improved addition help the multiplier to be generally faster.

ANALYSIS

The top diagram and RTL schematic diagram of 64x64 multiplier using Vedic mathematics are shown below figs 3 and 4. The inputs of the 64-bit multiplier are here a and b; the output is here too.

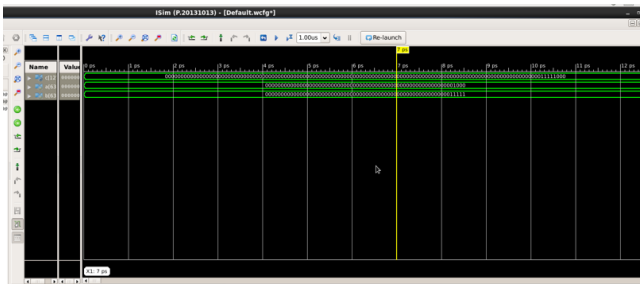


"Fig 3: Top Diagram"



"Fig 4: RTL Schematic"

The design capacity and structure of suggested layout are described by the above figures. Expanding the blocks helps us to find out the unique designs. The take a look at bench lets in one to confirm the outcome. figure five under displays a Xilinx tool result snapshot.



"Fig 5: Output Screenshot"

IV. RESULT

Designed using the Urdhva Tiryakbhyam sutra, the 64x64 Vedic multiplier displays a high-speed, low-electricity arithmetic unit suit for contemporary computational need. Its modular and hierarchical design makes scalability and incorporation into more large systems easier. The Vedic design greatly lowers device aid use, strength consumption, and time postpone whilst compared to conventional multipliers. these features make it a sturdy and flexible option for uses needing accurate and brief arithmetic operations, therefore organising it as a better substitute for current multiplier designs.

V. FUTURE SCOPE

We can amplify the concept in destiny by raising the bit count in terms of 2 power. i.e., 128, 256... As we know, the multiplier is a necessary module for digital photo and virtual signal processing programs; thus, we may utilise the present architecture as a module for ALU, convolution, MAC etc. Powerful multiplier layout raises the general application's efficiency.

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