Design of Optimal High-Frequency Wave Self-Mixing-VCO Architecture

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***Abstract*—One essential part of wired and wireless application systems is a voltage-controlled oscillator (VCO), for frequency conversion, it produces local oscillation signals, and for mixed-mode circuits, it produces fast clock signals. Recently, new millimeter-wave frequency-based high-speed wireless technologies have been created, implementing the LO signal in a synthesizer requires the use of a voltage-controlled oscillator (VCO) where the close-in phase noise is low and the oscillation frequency is high. In the millimeter-wave range, the VCO is essential for phase-locked loop (PLL) frequency control because it achieves a balance between frequency tuning range (FTR) and phase noise (PN). Communication systems running at GHz and higher frequency bands require the development of an on-chip local oscillator (LO) with a wide tuning range and outstanding spectral purity, LO (Local Osciallator) synthesis approaches must overcome a number of design challenges. To solve the above issues, design of optimal high-frequency wave self-mixing VCO architecture is presented. In order to achieve the required performance, in the Self-Mixing VCO (SMV), the first (f_0) and second ($2f_0$) harmonics are generated by the VCO core and combined.**

***Keywords*—Voltage Controlled Oscillator, Local Oscillator, Synthesis, Phase Noise (PN), Self-Mixer.**

I. INTRODUCTION

The functionality of portable electronic devices has advanced in recent years, moving toward small size and low power consumption, this is the process of combining several circuits and sensors into one chip. Low-cost power consumption, cheap cost, and as electronic devices transition to wireless control and low power, chip area reduction is an issue that needs to be addressed. Every wireless system, such as GSM, wireless sensor networks, WLAN, and Bluetooth, have the VCO circuit as their basic structure [1].

A VCO-based readout circuit applies the sensing core's output voltage to the VCO tuning voltage node, as opposed to an amplifier-based readout circuit, has the benefit of achieving a high signal-to-noise ratio and a low sensitivity level [2]. Furthermore, for the implementation of a large-scale sensor array, through the monitoring of the electromagnetic wave change between broadcast and received signals, the VCO-based readout circuit provides excellent integration and low power consumption, real-time remote detection of distance, velocity, and vital signs is possible with radar sensors. [3]. The PLL system, which is essential for communication systems, frequency synthesis, clock recovery, and high-speed digital circuits, this is the VCO gives systems like clock management and synchronization their initial timing.

Low phase noise properties in VCOs are necessary for a number of sensors that use them. Although frequency synthesizers, like the PLL, are commonly used to reduce phase noise, while the PLL's loop bandwidth in the frequency synthesizer is normally set to be between 100 and 500 kHz, the noise characteristics of the output signal of the synthesizer continue [4].

VCOs are among the most crucial components of frequency modulated DC-DC charge pump (CP) regulator systems, it takes a significant portion of the regulator's total energy usage into consideration [5]. In the low- to medium-frequency range, output frequency linearity over control voltage is more significant than phase noise, since relaxation-based VCOs perform worse in terms of phase noise, they are usually preferred over ring oscillators [6].

Particularly in modern multiband and wideband wireless communication applications, the transceiver characteristics and local oscillator signal are significantly impacted by the frequency band and VCO performance [7]. The highest frequency modulation curve can be obtained using the LC-tank VCO frequently features low parasitic capacitance effects and simple development. But a varactor pair's nonlinear capacitance variations result in a large variation in VCO gain, simplifies the process of developing a frequency synthesizer with phase noise performance and an identified loop bandwidth [8].

The low cost and high integration feature of VCOs make them significant when used in the CMOS process. For the most recent publications, in CMOS silicon technology, the VCO design is extremely popular. Consider to a number of VCO design requirements, such as tuning range, phase noise, and power dissipation [9].

The most crucial need for a good oscillator is phase noise, which is followed by sweep range, linearity, and distortion. Given that phase error, tuning range, higher frequencies come with trade-offs in terms of phase noise and power consumption, a CMOS differential oscillator with a large frequency range, low phase noise, it is challenging to provide low power and low phase error. [10].

Since they can match the necessary performance requirements, the best option for implementing millimeter wave circuits at the moment is nanoscale CMOS technologies, which provide system-on-chip (SoC) solutions that provide compactness and low cost. However, the technological scaling results in a large reduction in the supply voltage, this lowers power usage, making it advantageous for devices that run on batteries. [11]. However, it has an impact on the circuit voltage swing, which results in a number of disadvantages. In particular, this PN and tuning range must be traded off in millimeter wave applications are a lower power supply decreases both the oscillation amplitude and the VCO control voltage swing [12].

Through developing circuits based on inductor-capacitor (LC) tanks, these VCOs can be developed and the ring-based topology of complementary metal oxide semiconductors (CMOS). Higher operating frequencies and improved noise performance are maintained by LC tank-circuit VCO; however, since the inductor and capacitor require a large chip surface, the tuning range is reduced and parasitic capacitance is increased [13]. As an alternative, due to advancements in packaging density, the CMOS-based ring VCO offers a wider tuning range and does not require on-chip inductors. Voltage scaling is a widely used approach in VLSI circuits to reduce power dissipation. Furthermore, due to the fact that delay cells control voltage does not reach the whole power supply voltage range, a positive gate voltage is necessary to maintain the transistors in the appropriate working range. [14]. The VCO performs worse because of its limited output voltage swing. Research on CMOS VCOs with low power and large tuning range is challenging because design technologies are gradually being downscaled and low voltage operation with excessive integration is becoming more and more necessary [15].

Hence to solve the above mentioned issues, design of optimal high-frequency wave self-mixing VCO architecture is presented. The following is the manner the work is organized: The Literature Survey is described in Section II. The section III presents design of optimal high-frequency wave self-mixing VCO architecture. The results are analyzed in section IV, and the conclusion is presented in section V.

II. LITERATURE SURVEY

Lee Min-Chin and Shao-Qing Hong et. al., [16] describes the development of a voltage-controlled oscillator containing temperature sensors and a bandgap voltage reference source. A Bandgap reference Voltage circuit (BGRV) with a temperature-sensing VCO is proposed in this study, for use in wireless systems integrated circuits and low power management applications. The PTAT current and BJT V_{BE} are linearly combined to create the bandgap reference voltage source for this CMOS bandgap core reference voltage. Additionally, the VCO output frequency's linear temperature change is controlled by this PTAT voltage. The TSMC 0.35μm 2P4M process technology is used in the design and implementation of this suggested temperature sensor CMOS VCO with BGVR circuit. The chip has a

dimension of $0.750\times0.641mm^2$, a power dissipation of around 4.285 mW, and a temperature coefficient of approximately 11.14 ppm/°C and simulation and measurement results indicate that the operating temperature range is between 0°C and 100°C.

S. -F. Wang et. al., [17] shows that to use a single-ended delay cell to create a low-voltage, oscillator with full-swing voltage control and symmetrical even-phase values Additionally, it can use the suggested single-ended delay stage to obtain full-swing, even-phase outputs, a large tuning range, and lower supply voltage. Its simple structure also shows linear frequency-voltage characteristics and various output phases. At 12.6-48 MHz, a four-stage VCO was utilized to verify the proposed architecture, and at 1 MHz, the results revealed phase noise of -109.38 dBc/Hz. In a 0.18-μm RF CMOS process at a Taiwan semiconductor manufacturing company, the maximum power usage was around 1.8 mW in high-frequency mode and 1.2 mW in low-frequency mode at 1.2 V of the supply voltage.

Tang R., Gui X., Li D., Zhang Y., and Geng L. et. al., [18] provides an explanation of a gain variation compensation, or VCO, is a type of voltage-controlled ring oscillator. In order to reduce KVCO variation and nonlinearity through capacitive degeneration, a current-mode logic (CML) ring oscillator is suggested that uses a VCO with VCO-gain variation compensation. With a frequency range of 1.78 to 2.53 GHz and a gain change of less than 14.01%, Standard 0.18-μm CMOS technology was used in the design and construction of the suggested VCO. When using a 1.8-V supply voltage, it uses 20 mA, including the bias circuits,

and its central region is 0.185 x 0.081 mm². The high-band carrier frequency's phase noise, according to the tests, is -92.68 dBc/Hz at 1 MHz offset and -114.97 dBc/Hz at 10 MHz offset.

Kim H. -J., Kang S. -W., and Cho B. -H. et. al., [19] explains that to improve the dynamic performance of an LLC resonant converter through the use of an oscillator with adaptive voltage management. To improve the dynamic performance of LLC resonant converters, this work proposes an adaptive VCO. To efficiently regulate the LLC resonant converter's frequency response's low-frequency magnitude variation, the proposed adaptive VCO's frequency-dependent small-signal gains were developed. This results in enhanced dynamic performance across a wide range of operational circumstances. The suggested adaptive VCO has an easy formula and doesn't need any extra sensing circuits due to the approximated derivation. It is also robust to changes in circuit characteristics. Testing of the dynamic performance enhancement was done using a half-bridge LLC resonant converter prototype in the lab with a power output of 144 W.

Yu H., Chalamalasetty H. and Swaminathan M. et. al., [20] explains that to represent I/O- enhanced neural networks to control oscillators with dependent voltage. By including a periodic unit to provide the oscillation's phase information and to record the connection between the control signal and the instantaneous frequency, the suggested AugNNs predict the oscillatory output waveforms by using feed forward neural networks (FFNN). The VCOs with output buffers are modeled using an recurrent neural network (RNN)-based AugNN model that represents the output ports nonlinear dynamic current-voltage relationship. The suggested model is trained using transistor-level oscillator circuit simulation data. The suggested concept, which is a black-box technique, can be implemented in Verilog-A and protects

intellectual property (IP). The proposed model's effectiveness in time-domain analysis is demonstrated through examples of transistor-level oscillator circuits.

Masnadi Shirazi A. H. *et al*., [21] there was discussion of a mm-wave self-mixing-VCO design with a large tuning range and low phase noise. This paper presents an examination and performance comparison of fundamental-mode and harmonic-mode voltage-controlled oscillators (F-VCOs and H-VCOs). An H-VCO is shown to be able to simultaneously attain higher FTR and lower PN compared to a mm-wave F-VCO. To generate the self-mixing VCO (SMV), an H-VCO architecture, the required mm-wave third-harmonic (3fo) is created by combining the first (fo) and second (2fo) harmonics produced by the VCO core. In order to improve mixing efficiency, the VCO core's Class-C push-push architecture lowers parasitic capacitance, enhances the PN (phase noise) and the second-harmonic content. According to measurement data, at 1 MHz offset, the VCO achieves an FTR of 16.8% with a PN of -100.6 dBc/Hz while using 7.6 mW from a 1.2 V supply. The figure-of-merit (FoMT) that includes FTR is -190.85 dBc/Hz.

O. Esmaeeli *et al*., [22] explains a transformer-based technique for enhancing a self-mixing LCVCO functioning in terms of phase noise and tuning range at 20–28 GHz and 51–62 GHz. A 60 GHz self-mixing VCO with a 20 GHz core has a FoMT of -187.1 dBc/Hz, whereas a 65-nm CMOS VCO prototype with an FTR of 18.5% and a PN of -92.5 dBc/Hz at 1 MHz offset has a FoMT of -194.2 dBc/Hz and a PN of -107.9 dBc/Hz, and FTR of 29.9% for a 25 GHz VCO.

A. Nikpaik, Shirazi A. H. M., , Mirabbasi S. Molavi R. and Shekhar S. et. al., [23] provide an explanation of the millimeter-wave Class-C self-mixing VCO system's large tuning range and low phase noise. The self-mixing VCO (SMV) design generates the first (f 0) and second (f 0) harmonics using a Class-C push-push VCO topology. The two harmonics are then combined to produce the necessary third harmonic (3f 0). The SMV design performs better in the mm-wave spectrum in terms of phase-noise (PN) and frequency tuning range (FTR) than a fundamental-mode VCO running at 3f 0. A Class-C architecture reduces parasitic capacitance, phase noise, and mixing efficiency by increasing the second-harmonic content.

Vivek Jangra, Manoj Kumar, “IMOS varactor and multi-pass loop complementary current control are used in this wide tuning range VCO system for low power applications. A three-stage CMOS differential VCO with an IMOS varactor in the delay cell and the TSMC 180 nm CMOS technology was used to develop a complementary current control technique for multipass loops. Although complementary current control expels the control voltage limit, a traditional VCO is unable to manage the entire range of power source voltage. A power dissipation of 0.962 mW and control voltage swings between 1.0 V and 2.4 V are achieved using an IMOS varactor width of 5 μm and an oscillation frequency range of 5.460 GHz to 6.373 GHz are characteristics of the suggested differential ring VCO.

Dahiya, P.K., Yadav, R., & Mishra, R et. al., [25] explains that in order in order to develop effective high-frequency VCOs for automotive applications, this paper describes the design approach for a high-frequency CMOS VCO for long-range vehicle radio detection and ranging (RADAR), and simulation analysis is performed using the Cadence tool's Virtuoso SpectreRF program. For 45-nm CMOS technology, in the 24 GHz and 76 GHz frequency ranges, mm-wave CMOS current-starved ring and LC VCOs

function. Excellent performance is demonstrated by the suggested efficient VCO architecture for long-range automobile RADAR.

III. OPTIMAL HIGH-FREQUENCY WAVE SELF-MIXING

In this section, design of optimal high-frequency wave self-mixing VCO architecture is presented.

To generate a positive feedback loop, the VCO uses two pairs of PMOS and NMOS transistors that are differently cross-coupled. The cross-coupling topology is intended to offer enough feedback to achieve the required phase noise and oscillation frequency performance. To produce the required oscillation frequency and phase noise performance, the PMOS and NMOS transistor sizes are suitably selected. To guarantee optimal power consumption and linearity, the transistors' biasing conditions are carefully selected. The performance of the oscillator can be significantly impacted by parasitic elements like capacitance and resistance. These components may be involved in noise, frequency stability, and power consumption. These parasitic components must be carefully taken into consideration when designing and arranging the oscillator.

In addition to the differential output's fundamental (f_0), the common-mode output's second harmonic ($2f_0$) is likewise utilized by the Self-Mixing VCO. The $2f_0$ signal is a better implementation because its amplitude, this is higher than the $3f_0$ signal and can be obtained from a VCO. Additionally, the triple push VCO's high power consumption, single-ended operation, and strict matching criteria do not affect the SMV architecture.

Consider about an F-VCO and a 2H-VCO (harmonic mode VCO), both of which produces $2\omega_0$. The 2H-VCO's core oscillator runs at $\omega 0$ and employs an up-converter (such as a mixer) to reach $2\omega_0$. At ω_0, during the up-conversion process, the final output's PN is about 20 log(2) higher than the core oscillator's, assuming little AM to PM noise addition, the 2H-VCO's overall PN is lower than the F-VCO's PN, as demonstrated by PN theory, with the an excess PN provided by

$$PN_{excess} = 10\,log\left(\frac{R_{T,2\omega_0}}{R_{T,\omega_0}}\cdot\left(\frac{A_{\omega_0}}{A_{2\omega_0}}\right)^2\frac{(\Gamma_{T,rms,2\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,2\omega_0})^2}{(\Gamma_{T,rms,\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,\omega_0})^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{2\omega_0}}\right)^2\right) \quad (1)$$

In this case, R_T stands for tank parallel loss, A for oscillation amplitude, Γ_T,rms for RT noise's Impulse Sensitivity Function (ISF) rms values, Γ_T,rms-eff for the transistor's effective ISF [M1 or M2 thermal noise], and γ for a MOS transistor's excess noise factor. In (1), the subscripts ω_0 and $2\omega_0$ correspond the 2H-VCO and F-VCO cores, respectively, use these frequencies.

The$VCO\ FoM = PN + 10\log(P_{dc,mw}\cdot\left(\frac{\Delta f}{fo}\right)^2$ Utilizing power dissipation (measured in mW or dBm)-normalized Figure of Merit (FoM) for PN, an oscillation frequency, and an offset frequency, it is used to compare different oscillators, FoM_{excess} is characterized as

$$FoM_{excess} = FOM_{HVCO} - FOM_{FVCO} \approx PN_{excess}(Q,\Gamma,N) + 10\ log\left(\frac{P_{dc-FVCO}}{P_{dc-HVCO}}\right) \quad (2)$$

Define the RF power utilized by the tank as $P_{RF} = \frac{A^2}{R_T} = I_{RF,rms}\cdot V_{RF,rms}$ and $P_{dc} = I_{dc}\cdot$

For an NH-VCO with an output frequency of $N\omega_0$ and an up-conversion ratio of N, V_{dc} (2) can be simplified. (2) can be generalized as

$$FOM_{excess}(Q,\Gamma,N) = 10\log\left(\left(\frac{\eta_{V,\omega_0}\cdot\eta_{I,\omega_0}}{\eta_{V,N\omega_0}\cdot\eta_{I,N\omega_0}}\right)\left(\frac{(\Gamma_{T,rms,N\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,N\omega_0})^2}{(\Gamma_{T,rms,\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,\omega_0})^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{2\omega_0}}\right)^2\right)\right.$$

where the voltage and current efficiencies are represented by ηV and ηI. According to equation (3), FoM_{excess} is dependent on ISF, Q, and device efficiency (e.g., voltage and current efficiency).

For 2H-VCO is

$$FOM_{excess}(Q,\Gamma,N) = 10\log\left(\left(\frac{\eta_{V,\omega_0}\cdot\eta_{I,\omega_0}}{\eta_{V,N\omega_0}\cdot\eta_{I,N\omega_0}}\right)\left(\frac{(\Gamma_{T,rms,2\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,2\omega_0})^2}{(\Gamma_{T,rms,\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,\omega_0})^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{2\omega_0}}\right)^2\right)\right. \quad (3)$$

First, if the signal swing produced by the F-VCO (Fundamental) and NH-VCO cores is same ($\eta_{V,\omega 0} = \eta_{V,N\omega 0}$), it should be mentioned that if $A\omega_0 = AN\omega_0$, the F-VCO may use more current, primarily because of lower passive quality factors and a decline in device efficiency. Assuming this, FOM_{excess} can be reduced to

$$FOM_{excess}(Q,T) = 10\log\left(\left(\frac{\eta_{I,\omega_0}}{\eta_{I,N\omega_0}}\right)\left(\frac{(\Gamma_{T,rms,N\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,N\omega_0})^2}{(\Gamma_{T,rms,\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,\omega_0})^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{2\omega_0}}\right)^2\right)\right. \quad (4)$$

Second, L is set to be inversely proportional to ω_0 if RT is proportionate to Q (RT = LQ ω_0, for example), and Since $I_{dc\text{-}\omega 0} = I_{dc\text{-}N\omega 0}$, equal amounts of power are used by the NH-VCO and F-VCO cores, $\approx \eta_I I_{dc} R_T$,FOM_{excess} can be simplified as

$$FOM_{excess}(Q,T) = 10\log\left(\left(\frac{\eta_{I,\omega_0}}{\eta_{I,N\omega_0}}\right)^2\left(\frac{(\Gamma_{T,rms,N\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,N\omega_0})^2}{(\Gamma_{T,rms,\omega_0})^2+(\gamma\Gamma_{T,rms,-eff,\omega_0})^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{2\omega_0}}\right)^3\right)\right. \quad (5)$$

Using in 20 and 40 GHz, respectively, the structure generates f_0 and $2f_0$ components in the first stage of a class-c push-push VCO. In the second step, the f_0 and $2f_0$ components are combined using a single-balanced active mixer, which produces the necessary LO component at $3f_0$ at the mixer's output.

IV. RESULT ANALYSIS

In this section, design of optimal high-frequency wave self-mixing VCO architecture is presented. The Figure 1 shows the layout diagram of presented optimal high-frequency wave self-mixing VCO architecture.

Fig. 1. Layout Diagram of optimal high-frequency wave self-mixing VCO

The output waveform of the VCO model is displayed in Figure 2.

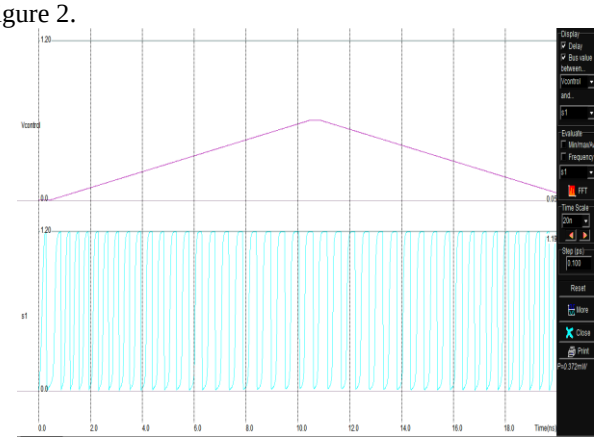

Fig. 2. Output Waveform

The Figure 3 describes the power consumption comparison.

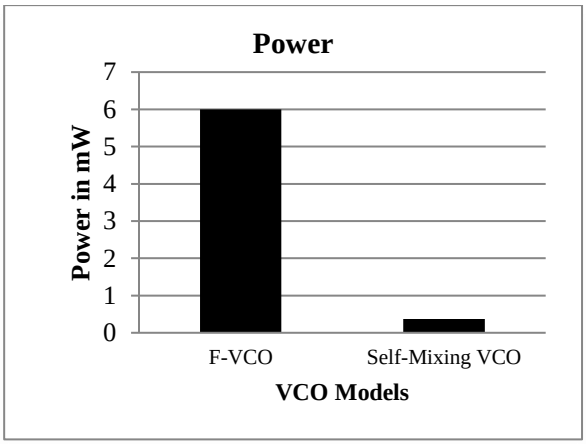

Fig. 3. Power Consumption

In Figure 3, the x-axis indicates the VCO models while the y-axis indicates the power consumption in milli Watts (mW). Compared to Fundamental VCO (F-VCO), presented VCO has consumed very less power. The Figure 4 shows the FTR comparison between self mixing VCO and F-VCO.

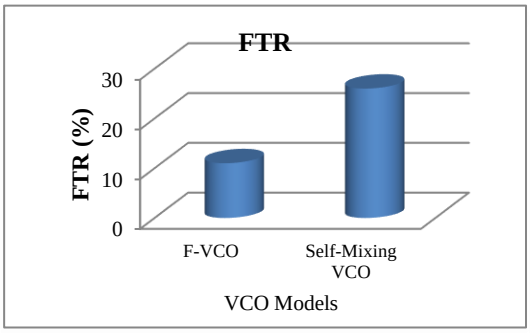

Fig. 4. FTR Performance

In Figure 4, the x-axis represents the VCO models while the y-axis indicates the FTR in terms of percentage. The self-mixing VCO has better FTR than F-VCO model. Hence this model has exhibited better FTR and power consumption performance.

V.CONCLUSION

In this Analysis, design of optimal high-frequency wave self-mixing VCO architecture is presented. The first (f_0) and second (ff0) harmonic are produced by the VCO core, which then combines them to produce the necessary mm-wave third harmonic ($3f_0$) in a self-mixing VCO (SMV) H-VCO design. Despite the triple push VCO's high power consumption, in order to reduce spurious components at the lower mixing sideband and improve frequency selectivity, the mixer is tuned at $3f_0$, and strict matching criteria are not problems with this SMV architecture. The offered VCO's performance is verified using FTR and power consumption. The provided model performs better than the F-VCO.

Simulations and analyses verify that the technique's tuning range is better than that of direct synthesis methods.

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